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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,742	12/16/2003	Jae-Eun Lim	P69388US0	3669

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,742	LIM ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 6-20* is/are rejected.

7)☒ Claim(s) *2-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/16/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 12/16/03. Currently, claims 1-20 are pending.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 12/16/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The disclosure is objected to because of the following informalities:

On page 6, line 11, "gate oxide 215" should read "gate oxide 218".

On page 10, line 5, "pad nitride 316" should read "pad nitride 314".

On page 15, line 22, "pad nitride 416" should read "pad nitride 414".

Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-8, 11, 13-16, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyer et al. US Patent 6,498,383 in view of Wu et al. US Patent 6,180,467.

Beyer discloses the semiconductor method substantially as claimed. See figures, 1-8, and corresponding text, where Beyer shows, pertaining to claims 1 and 14, a method for manufacturing a shallow trench isolation (STI) in a semiconductor device, the method comprising the steps of: a) preparing a semiconductor substrate **3** obtained by a predetermined process, on which a pad oxide **5** and a pad nitride **7** are formed on predetermined locations thereof (figure 1; col. 3, lines 27-31); b) forming an isolation trench **11** with a predetermined depth in the semiconductor substrate (figure 1); c) forming a wall oxide **13** on the trench (figure 1; col. 3, lines 40-43); e) (claim 1) carrying out a nitridation process for forming a nitrided oxide **27** or d) (claim 14) carrying out a nitridation process for forming a nitrided oxide on the wall oxide (figure 5; col. 4, lines 41-67; col. 5, lines 1-6); f) forming an insulating layer **29** over the resultant structure, wherein the isolation trench is filled with the insulating layer (figure 6; col. 6, lines 16-30); and g) planarizing top face of the insulating layer (col. 6, lines 55-59).

Also, Beyer shows, pertaining to claims 7 and 15, the method wherein the steps e) (claim 1) and d) (claim 14) are carried out by using a remote plasma nitridation (RPN) (col. 5, lines 7-29). Beyer shows, pertaining to claims 8 and 16, the method wherein the steps of e) (claim 1) and d) (claim 14) are carried out by using an N_2 gas diluted with helium (He) as the source gas at the temperature in the range of about 550 °C to about 900 °C (col. 4, lines 58-61; col. 5, lines 10-18, ***Note***: helium is an inert gas. See Periodic Table under Group VIII). Finally, Beyer shows, pertaining to claims 13 and 20, the method wherein the step of f) is carried out by using a

material selected from the group consisting of a high density plasma (HDP) oxide, an advanced planarized layer (APL) and a spin on dielectric (SOD) (col. 6, lines 24-54).

However, Beyer fails to show, pertaining to claims 1 and 14, the steps of d) and e), respectively, forming a liner oxide on the wall oxide and an exposed surface of the pad nitride (claim 1) or on the nitrided oxide (claim 14). In addition, Beyer fails to show, pertaining to claim 6, the method wherein the step e) is carried out by using a plasma process, thereby forming the nitrided oxide on the liner oxide. Finally, Beyer fails to show, pertaining claim 11, the method wherein the step d) is carried out by repeating a chemical vapor deposition (CVD) process for forming a plurality of interfaces on the wall oxide

Wu teaches in figures 1A-1E, and corresponding text, pertaining to claims 1, 6, 11 and 14, a similar method for manufacturing shallow trench isolation (STI), having a trench isolation region that includes a liner oxide film on the wall oxide and the pad nitride film (col. 3, lines 10-23).

It would have been obvious to one of ordinary skill in the art to substitute, forming a liner oxide on the wall oxide and exposed surface of the pad nitride or on the nitrided oxide, in the method of Beyer, pertaining to claims 1, 6, 11 and 14, according to the teachings of Wu, with the motivation that, the additional liner layer is used as a barrier layer to prevent elements from the filler oxide layer and subsequent layers from diffusing into the active regions. In addition, one of ordinary skill in the art would be drawn to the use of an additional liner oxide layer over the wall oxide or the nitrided oxide, to further enhance protection to the silicon substrate against out-diffusion and contamination resulting from further processing techniques. Finally, it would have been obvious to form the liner oxide film by chemical vapor deposition (CVD) process for

forming a plurality of interfaces on the oxide wall since this process is well known in the conventional art of deposition techniques.

Claims 9, 10, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyer et al US Patent 6,498,383 in view of Wu et al. US Patent 6,180,467 in further view of Ohmi et al. US Patent 6,669,825.

Beyer in view of Wu shows the semiconductor method substantially as claimed. See the previous 35 U.S.C. 103(a) rejections, pertaining to claims 1, 6-8, 11, 13-16, and 20.

However, Beyer in view of Wu fails to show, pertaining claims 9 and 17, the method wherein the steps e) and d), respectively, are carried out by using a radial line slot antenna (RLSA). In addition, Beyer in view of Wu, fails to show, pertaining to claims 10 and 18, the method wherein the steps e) and d), respectively, are carried out by using a mixture gas of an argon gas, an N_2 gas and an O_2 gas as the source gas at the temperature in the range of about 150 °C to about 600 °C.

Ohmi teaches, in figures 1-26 with emphasis on figures 2 and 11B, and corresponding text, pertaining claims 9, 10, 17 and 18, the use of a microwave plasma processing apparatus that uses a radial line slot antenna to form a high quality oxynitride film including a mixture gas of an argon gas, an N_2 gas and an O_2 gas as the source gas at the temperature in the range of about 550 °C or less, for the purpose of forming an improved insulation film (col. 3, lines 1-4; col. 6, lines 55-67; col. 7, lines 16-34; col. 10, lines 59-65; col. 11, lines 1-19).

It would have been obvious to one of ordinary skill in the art to carry out, the steps of e) and d) in claims 1 and 14, respectively, by using a radial line slot antenna (RLSA) and, to

include using a mixture gas of an argon gas, an N_2 gas and an O_2 gas, as the source gas at the temperature within the range of about 150 °C to about 600 °C, in the method of Beyer in view of Wu, pertaining to claims 9, 10, 17 and 18, according to the teachings of Ohmi, with the motivation that, the microwave plasma processing apparatus includes a radial line slot antenna (RLSA), resulting in the formation of a high-quality insulation film, such as an oxynitride film formed by a mixture gas of an argon gas, an N_2 gas and an $O_{2,}$, that will not cause substantial leakage of current. In addition, the apparatus including (RLSA), provides a faster and very uniformed film forming process. Also, the apparatus including (RLSA), eliminates plasma damage to the substrate, due to the high-density plasma formed by microwave excitation, that results in a low electron temperature and plasma potential at the surface of the substrate. Furthermore, since there is an absence of plasma sputtering in the processing chamber of the apparatus including (RLSA), the problem of contamination to the substrate is eliminated. Therefore, it would be obvious to one of ordinary skill in the art to use a microwave plasma processing apparatus including a (RLSA), to form a more efficient nitrided oxide insulation film on the wall oxide within the trench of the substrate.

Claims 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beyer et al. US Patent 6,498,383 in view of Wu et al. US Patent 6,180,467 in further view of *Stanley Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, Lattice Press, Second Edition, 2000.*

Beyer in view of Wu shows the semiconductor method substantially as claimed. See the previous 35 U.S.C. 103(a) rejections, pertaining to claims 1, 6-8, 11, 13-16, and 20.

However, Beyer in view of Wu, fails to show, pertaining to claims 12 and 19, the method wherein the step c) is carried out by using dry oxidation process on the condition that a process temperature is in the range of about 850 °C to about 900 °C and a chlorine gas is supplied with amount in the range of about .1% to about 10%.

Wolf teaches, on pages 277-283, conventional dry oxidation techniques including the advantages of using chlorine within a dry oxidation process, that includes performing the dry oxidation process under the condition that the process temperature is in the range of about 850 °C to about 900 °C and a chlorine gas is supplied with an amount in the range of about .1% to about 10%.

It would have been obvious to one of ordinary skill in the art to incorporate, the method wherein the step c) is carried out by using dry oxidation process on the condition that a process temperature is in the range of about 850 °C to about 900 °C and, a chlorine gas is supplied with the amount in the range of about .1% to about 10%, in the method of Beyer in view of Wu, pertaining to claims 12 and 19, according to the teaching of Wolf, with the motivation that, during conventional dry oxidation, the chlorine gas is introduced as part of the oxidation cycle, which causes an increase in the oxidation rate and an improvement to the material properties of the oxide. Therefore, it would be obvious to one of ordinary skill in the art to use a dry oxidation process that includes a chlorine gas to form a wall oxide within the trench, based on the well known conventional art of dry oxidation techniques. In addition, the temperature range of about 850 °C to about 900 °C and, a chlorine gas supplied with the amount in the range of about .1% to about 10%, is considered to be within conventional specifications, especially since no criticality has been shown.

Allowable Subject Matter

Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or render obvious the method "...thereby forming the nitrided oxide between the liner oxide and the wall oxide."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
September 3, 2004

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